

Advanced SoC Architectures for Embedded Systems
(Graduate Course, Fall 2009)

Professor: Dr. Sungjoo Yoo, sungjoo.yoo@postech.ac.kr

Office: Engineering Building #2, 417

Classroom, day & time: Eng. Bldg 2-106, Mon/Wed, 13:15~14:45

1. Course Description

Design issues of advanced system-on-chip (SoC) architectures for embedded systems are explained and discussed with particular emphasis on memory hierarchy including cache, DRAM and SSD (solid state disk), and on-chip network.

2. Course Prerequisites

Microprocessor and digital logic design, computer architecture (undergraduate course)

3. Grading

Mid-term exam: 25%, final exam: 25%, paper presentation: 20%, practices & term project: 30%

4. Examination

Mid/final exam: open book

5. Practices & Paper Presentation

The practices in this course are to help students to understand and experience the key lessons discussed in this lecture.

Each student needs to select one paper among the reading paper list (to be provided later), prepare slides summarizing the key contents of the papers, and present them in the class.

6. Course Text

Main Text Books

“Memory Systems: Cache, DRAM, Disk”, B. Jacob, 2007

“Principles and Practices of Interconnection Networks”, W. Dally and B. Towles, 2004.

Recommended Readings

“The Art of Multiprocessor Programming”, M. Herlihy, 2008

“Computer Architecture”, 4th Ed., J. Hennessy and D. Patterson, 2007

"Parallel Computer Architecture", D. Culler and J. Pal Singh, 1999.

“Chip Multiprocessor Architecture”, K. Olukotun, L. Hammond, and J. Laudon, Morgan & Claypool, 2007.

Technical papers at ISCA/HPCA/MICRO/ISSCC/DAC/ICCAD/DATE/ASPDAC/CODES, etc.

Technical reference manuals, e.g. ARM technical documents for AXI protocol, PL301/34x, etc.

(URL's to all the technical papers will be provided on the class web site.)

7. Lecture Schedule

Visit the class web site at <http://cal.postech.ac.kr/2009/EECE695R.htm>

| Lecture Title | Practices & Notes |
|--|---|
| Class Introduction (9/2) | |
| Instruction Level Parallelism & Thread Level Parallelism (9/7, 9/9) | |
| Introduction to Parallel Programming (with CUDA on GPU) and Synchronization (9/14, 9/16) | |
| CUDA Programming Practice (9/17~18) | Practice #1 to be done by nVidia Korea |
| Cache (9/21, 9/23, 9/28) | Practice #2 Cache simulation - Cache size vs. miss ratio - Prefetch effects |
| DRAM (9/30, 10/5, 10/7) | Practice #3 DDR memory simulation - Effects of memory access scheduling and # memory channels |
| No Classes (10/12, 14) | Prof. Yoo attends ESWEEK2009 Submission of two reports on Practices #2 and #3 by 10/18 |
| Mid-term exam (10/19, night) | |
| Network-on-Chip (10/21, 10/26, 11/2, 11/11) Maybe no class on 11/9 (Graduate entrance exam) | Practice #4 NoC simulation - 6x6 NoC model - Effects of speculative, lookahead, and EVC Submission of report on Practice #4 by 11/25 |

| | |
|---|--|
| No Classes (11/16, 11/18) | Prof. Yoo attends SEUS2009 |
| HDD, SSD (11/25, 11/27) | |
| Seminar Sessions (12/2, 12/4, 12/9, 12/11) | 20~30min presentation + 10min Q&A per paper |
| Final Exam (12/16) | Covering both lectures and paper presentations |

Note: Supplementary classes (9/17~18, CUDA practice, 8 hours) will compensate for the lost 5 classes on 10/12, 10/14 (CODES conference), 11/9 (Graduate entrance exam), and 11/16, 11/18 (SEUS 2009).